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(12) # EUROPEAN PATENT APPLICATION

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(54) **Semiconductor wafer array.**

(57) A semiconductor wafer array comprising a plurality of wafers (10-18) of semiconductor material. Each of the wafers (10-18) is provided with cone-shaped or pyramid-shaped vias (25). Inserted in each of the vias (25) is a correspondingly shaped wad of electrically conductive compliant material for foaming continuous vertical electrical connections between the wafers (10-18) in the stack. The base of each wad makes connection to a bonding pad (32-37) on the surface (30) of a lower wafer (10-18) as well as to the electrically conductive compliant material in the lower wafer (10-18).

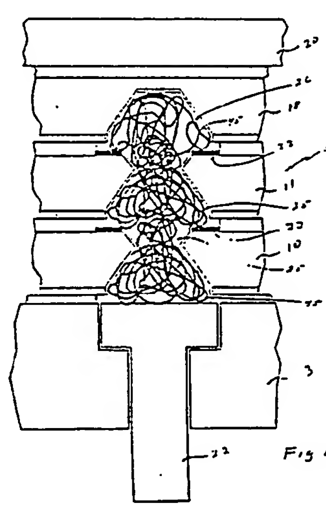


Fig 12

EP 0 314 437 A1

Description

SEMICONDUCTOR WAFER ARRAY

The present invention relates to semiconductor wafer arrays in general and in particular to a method and apparatus comprising a stacked array of semiconductor wafers which are vertically interconnected by means of a plurality of wads of an electrically conductive compliant material.

Since the development of integrated circuit technology, computers and computer storage devices have been made from wafers of semiconductor material comprising a plurality of integrated transistor circuits.

It is desirable to use complete wafers in data processing equipment. The individual circuits may be removed from the wafer on chips of semiconductor. The circuits can then be connected together whilst mounted on a circuit board. However, a large amount of wiring will be needed to produce a data processing unity. If the individual circuits on the wafer are wired together whilst still part of the wafer a more compact unit, with a faster response, is obtained. This may be achieved using wafer scale integration (WSI) techniques. However, the practical difficulties of producing large, unflawed, semiconductor wafers means that generally a plurality of wafers need be used. To save space these are generally stacked one above another within the data processing device.

Attempts to avoid the disadvantages of interconnecting a plurality of stacked wafers using wires have involved large scale parallel array processors and memory devices in which parallel circuit members are interconnected using vertical columns of solid, dense conductive material such as solder, copper, etc. For example, in U.S. Patent No. 4,368,106 and in U.S. Patent No. 4,394,712.

Alternatively, a vertical column may be filled with an electrically conductive compliant material, such as wads of fine wire, in a similar way to that used to connect a stack of circuit boards. This is disclosed by U.S. Patents Nos. 4,574,331 and 4,581,679. U.S. Patent No. 4,029,375 discloses an alternative type of connector for connecting a vertical stack of printed circuit boards.

In view of the foregoing, principal objects of the present invention are a method and apparatus comprising a semiconductor wafer array in which the individual wafers in the array, as distinguished from printed circuit boards, are stacked one on top of another and vertically electrically interconnected using an electrically conductive compliant material such as a wad of fine wire or a wad of electrically conductive elastomer.

In accordance with the above objects, each wafer in the array is provided with one or more vias, as by chemical or laser drilling or the like. After the walls of the vias in the wafers are coated with a layer of electrically insulating material, the vias are filled with wads of electrically conductive compliant material and the wafers are stacked one on top of another.

The shape of the vias and the wads are important features of the present invention. In order to eliminate the necessity for a separate means for holding the individual wads of electrically conductive compliant material in position and to provide vertical electrical connections between wafers as well as lateral electrical connections to electrical circuits on each of the wafers, the vias and wade are formed with inwardly sloping walls having an overall cone, hourglass or pyramid shape. A ring-shaped electrical pad which is electrically laterally connected to circuits on a wafer is provided surrounding the apex or small end of the vias as needed. The apex or small end of the wads is formed to project beyond the apex of the vias and the "base or large end" of the wads is formed to project beyond the base of the vias. When a stack of such wafers is formed the apex of a wad is compressed into the base of a wad in a wafer adjacent thereto. At the same time the base of the latter wad is compressed against the electrically conductive ring-shaped pad thus forming both a vertical electrical connection to an overlying wafer as well as to the electrical circuits connected to the pad.

In the process of fabricating an array, the wafers are oriented with the apex of cone-shaped or similarly shaped vias facing downwardly. Cone-shaped or similarly shaped wads of electrically conductive compliant material are then placed in the vias. Because of their respective shapes, the wads are prevented from falling out of the vias so long as the wafers are not turned over. After all of the vias in the wafers are loaded with the wads, the wafers are stacked together and placed on a base plate.

The base plate is fitted with a plurality of electrical feedthrough pins which make contact with the base of the wads of electrically conductive compliant material in the lowest one of the wafers in the array. The wafer at the top of the stack is provided with a pressure applying member so as to press all of the wafers together, thereby compressing the individual wads of electrically conductive compliant material together as described above. As will be appreciated wafers may be added to or removed from the stack as required and the over-all change in the size of the stack merely corresponds to the thickness of the wafer involved.

The above and other objects, features and advantages of the present invention will become apparent from the following detailed description of the accompanying drawing, in which:

Fig. 1 is a cross-sectional view of a semiconductor wafer array comprising a plurality of stacked wafers according to the present invention;

Fig. 2 is a plan view of one of the wafers of Fig. 1 showing several ring-shaped electrical pads on one surface thereof;

Fig. 3 is a cross-sectional view taken in the direction of lines 3-3 of Fig. 2;

Fig. 4 is a cross-sectional view showing the wafer of Fig. 3 after it has been coated with an etch-resistant material;

Fig. 5 is a cross-sectional view of the wafer of Fig. 4 after it has been patterned to expose a square area on the backside of the semiconductor wafer substrate beneath the pads;

Fig. 6 is a cross-sectional view of the wafer of Fig. 5 showing two through-holes provided therein;

Fig. 7 is an enlarged cross-sectional view of one of the vias shown in Fig. 6 after the etch-resistant coating shown in Figs. 4-6 is removed from the center of the ring-shaped pad surrounding the via.

Fig. 8 is a cross-sectional view of the via of Fig. 7 after the sharp edges at the apex of the via are removed;

Fig. 9 is a cross-sectional view of the via of Fig. 8 after its walls have been coated with an electrically insulating layer.

Fig. 10 is a cross-sectional view of the via of Fig. 9 after the etch-resistant coating shown in Figs. 4-9 is removed from the ring-shaped pad.

Fig. 11 is a cross-sectional view of the via of Fig. 10 after a wad of compliant electrically conductive fine wire is inserted therein;

Fig. 12 is an enlarged partial cross-sectional view showing two wafers stacked one on top of another between a dummy wafer and a base plate with the wad of Fig. 11 inserted in each of the vias located therein according to the present invention;

Fig. 13 is an enlarged partial cross-sectional view showing an alternative embodiment of the present invention, comprising electrically conductive compliant elastomeric material;

Fig. 14 is an alternative embodiment of the present invention showing the top of a wad of fine wire compressed onto the pad surrounding the via; and

Fig. 15 is a partial cross-sectional view showing relative dimensions of the vias in the wafers.

Referring to Fig. 1, there is provided in accordance with the present invention a semiconductor wafer array designated generally as 1. In the array 1 there is provided a housing 2 mounted on a base plate 3. In the housing 2 there is provided a plurality of side walls 4, 5 and 6 and a top wall 7. A front wall corresponding to side walls 4-6 is not shown. Located in the housing 2 between the base plate 3 and top wall 7, there is provided a stack of semiconductor wafers 10-18. In the stack of wafers 10-18, the bottom wafer 10 is located adjacent to the base plate 3. The top wafers 18 is located nearest to the top wall 7. Wafer 18 may be a dummy wafer which is used simply for terminating the vertical electrical connecting members and forming an electrical connection with the pads on wafer 17 as will be further described below. On top of wafer 18 between wafer 18 and top wall 17, there is provided a compliant electrically insulating thermally conductive pad 20. Pad 20 is located between the wafer 18 and the top wall 7 to compensate for thermal expansion and contraction of the stack of wafers 10-18 and for conducting heat from the stack of wafers 10-18 to the top wall 7. Extending from the top wall 7 there is provided a plurality of metallic fingers 21. Fingers 21 comprise cooling fins for dissipating heat from the housing 2.

Extending through the base plate 3 there is provided a plurality of electrical pin members 22. Pin members 22 are provided for making electrical contact with electrically conductive compliant material in vias in the stack of wafers 10-18, as will be further described below.

In practice, the base plate 3 comprises insulating material, such as ceramic material, for insulating the pin members 22 from each other, and the side wall members 2 and 4 may comprise a metallic material. The free area within the housing 2 may be filled with a conventional electrically non-conductive gaseous or liquid material to facilitate the dissipation of heat from the housing 2.

In each of the wafers 10-17 there is provided a plurality of hourglass-shaped vias 25. Corresponding pyramid-shaped recesses 26 are normally provided in dummy wafer 18. In each of the vias 25 and recesses 26 there is provided a wad 27 of an electrically conductive compliant material, such as, for example, a fine wire or an electrically conductive elastomer. The vias 25 and recesses 26 in the wafers 10-18 are placed in registration with a corresponding via in an adjacent wafer, such that the wads 27 of electrically conductive compliant material in the vias combine to form a conductive vertical column providing electrical connections from feedthrough pins 22 to each of said semiconductor wafers 10-18.

While the embodiment of Fig. 1 shows a sealed housing 2, it is understood that conventional ports for circulating cooling gases or fluids may be added to the housing 2 in a manner as best fits the heat flow requirements of the application circuits located therein. Also, in certain applications, certain of the vias 25 may provide vertical connections between two or more but less than all of the wafers.

Referring to Figs. 2-11, the steps used for fabricating each of the semiconductive wafers in the stack of wafers 10-18 will now be described. For convenience, the description will be made with respect to wafer 10, it being understood that the other wafers 11-17, except for possible differences in the electrical circuits provided therein, are substantially identical insofar as the present invention is concerned.

Referring to Figs. 2 and 3, wafer 10, a 1,0,0 silicon wafer, is provided with a first or topside surface 30 and a second or backside surface 31. Electrical circuits, e.g. logic circuits, memory cells, or the like (not shown), are provided in the surface 30 and laterally electrically connected to one or more ring-shaped pads 32-37. While only 6 pads are shown, it is to be understood that many such pads are normally present on each wafer.

The surfaces 30 and 31 of the wafer 10 are then provided with a coating 34 of etch-resistant material such as silicon nitride as shown in Fig. 4. After the wafer 10 has been coated with the etch-resistant material, the coating 34 is patterned on the backside 31 of the wafer 10 by techniques known in the microlithographic art and plasma-etched so as to provide square openings 35 in the nitride coating

exposing the wafer 10 beneath the pads 32-37 as shown in Fig. 5. After the square openings 35 are produced, the wafer 10 is subjected to a conventional anisotropic etch process,such as 85° C potassium hydroxide at 35% concentration, that produces a truncated pyramid-shaped hole or recess 36 in the wafer 10 as shown in Fig. 6. Other techniques may also be used for fabricating the holes 36 such as those comprising laser means and combined laser and etch means. Any means that yields roughly pyramid-, cone- or hourglass-shaped vias, while avoiding damage to the surface of the wafer, may be used for the purpose of this invention.

Referring to Fig. 7, there is shown an enlarged cross-sectional view of the pad 33 and hole 36 in the wafer 10. As shown in Fig. 7, the anisotropic etch process used for making the holes 36 as described above with respect to Fig. 6 produces extremely sharp and therefore somewhat fragile edges 37 which are subject to chipping and cracking. In order to remove the sharp edges 37, the silicon nitride coating 34 in the center of the pad 33 is removed and the wafer 10 subjected to a second short anisotropic etching process. This etching process produces a second inverted truncated pyramid-shaped hole 38, thus forming square-sided hourglass-shaped vias 25 as shown in Figs. 1 and 8.

After the vias 25 are formed in the wafer 10, an insulating layer 40 of silicon nitride is grown or deposited on the walls of the vias 25 so as to provide electrical isolation of the wafer 10 as shown in Fig. 9. Thereafter, the silicon nitride coating 34 is removed from the bonding pad 33 as shown in Fig. 10. For the purpose of this disclosure, it may be assumed that the wafers 10-18 are approximately 0.448mm thick, that the aperture 41 at the top of the via 25 is approximately 0.224mm on a side and that the aperture 42 at the bottom of the via 25 is approximately 0.672mm on a side.

Referring to Fig. 11, there is provided in each of the vias 25 a wad of electrically conductive compliant material 45. In one of the embodiments of the present invention, the wad 45 comprises a wad of single strand fine wire. The shape of the wad 45 is roughly that of a pyramid or a cone. The diameter of the wire used to make the wad 45 is approximately 1/10th that of the width of the top side aperture 41, i.e. 0.022mm and the volume of the wire used is such as to fill the vias 25 to within 10 to 20% of their volume; the remainder of the via volume comprising the air space between the wire in the wad. Any suitable conventional means may be used for pre-forming the wads 45 into the desired shape.

Referring to Fig. 12, there is shown an assembly 50 comprising three of the wafers 10-18, namely wafers 10, 11 and 18, having vias 25 and 26, each containing a wad of compliant fine wire as described above with respect to Fig. 11. The wafers 10, 11 and 18 are supported on the base 3 with the vias 25 and 26 in each of the wafers located in registration with one of the feedthrough pins 22 in the base 3. Located on top of the stack of wafers 10, 11 and 18 there is also provided the thermally conductive pad 20 described above with respect to Fig. 1. The wafers 10, 11 and 18 may also contain through-holes for the purpose of receiving alignment pins (not shown) for holding the vias in the wafers in alignment. Of course, other means may also be used for keeping the wafers in alignment.

The configuration of the vias 25 and 26 and the wads 45 as shown in Figs. 11 and 12 is an important feature of the present invention. The pyramid or cone shape of each of the wads 45 allows its base or larger end to make connection to the wafer bonding pad 33 while its apex or smaller end makes connection to the base of the next higher vertical wad 45. In the case of the bottom wafer 10, the base of the wad 45 therein makes an electrical contact with the feedthrough pin 22, as also shown in Fig. 1. In the case of the top dummy wafer 18, the dummy wafer 18, without circuits, is used as a containment for the top level of wads 45 so as to compress the wads and provide an electrical connection to the pad 33 on the topmost circuit wafer 11 and the underlying wad 45 in the wafer 11.

As an alternative to the fine wire wads 45 of Fig. 12, Fig. 13 shows a shaped form of conventional compliant conductive elastomer 51. A plurality of wads 51 may be used in place of wads 45 if desired.

Referring to Fig. 14, there is provided in an alternative embodiment of the present invention a wad of electrically conductive compliant wire material 55. Wad 55 is substantially identical to wad 45 described above with respect to Figs. 11 and 12 with the exception that the wad 55 is made to extend through the wafer 10 and a portion 56 thereof is then compressed back against the bonding ring pad 33 so as to cause the wafer to retain the mass of fine wire 55 in the vias 25 and to insure contact to the bonding ring 33. This configuration may be used in place of the wads 45 used in wafer 10-17 and, if used in wafer 17 at the top of the stack, the use of the dummy wafer 18 to insure the making of an electrical contact to the pad 33 on the wafer 17 may be avoided.

Referring to Fig. 15, the width s2 of the vias 25 is given by the equation

$$s2 = s1 + \sqrt{2}\, t - 2\sqrt{2}\, rt$$

where

s1 is the width of the apex of the vias 25,
t is the thickness of the wafer 10 and
r is a constant having a value less than unity, (e.g. .1 - .2.)

While several embodiments of the present invention are described above, it is contemplated that various modifications may be made thereto without departing from the spirit and scope of the present invention. For example, the second etch described above for making the hole 38 may be an isotropic etch thereby producing the same sized hole but with parallel sidewalls. Of course, the wads 45 may be similarly shaped. In all cases, the methods and means used for forming the vias and the wads comprise conventional semiconductor wafer processing techniques. Accordingly, it is intended that the embodiments described be considered only as illustrative of the present invention and that the scope thereof should not be limited thereto but be determined by reference to the claims hereinafter provided and their equivalents.

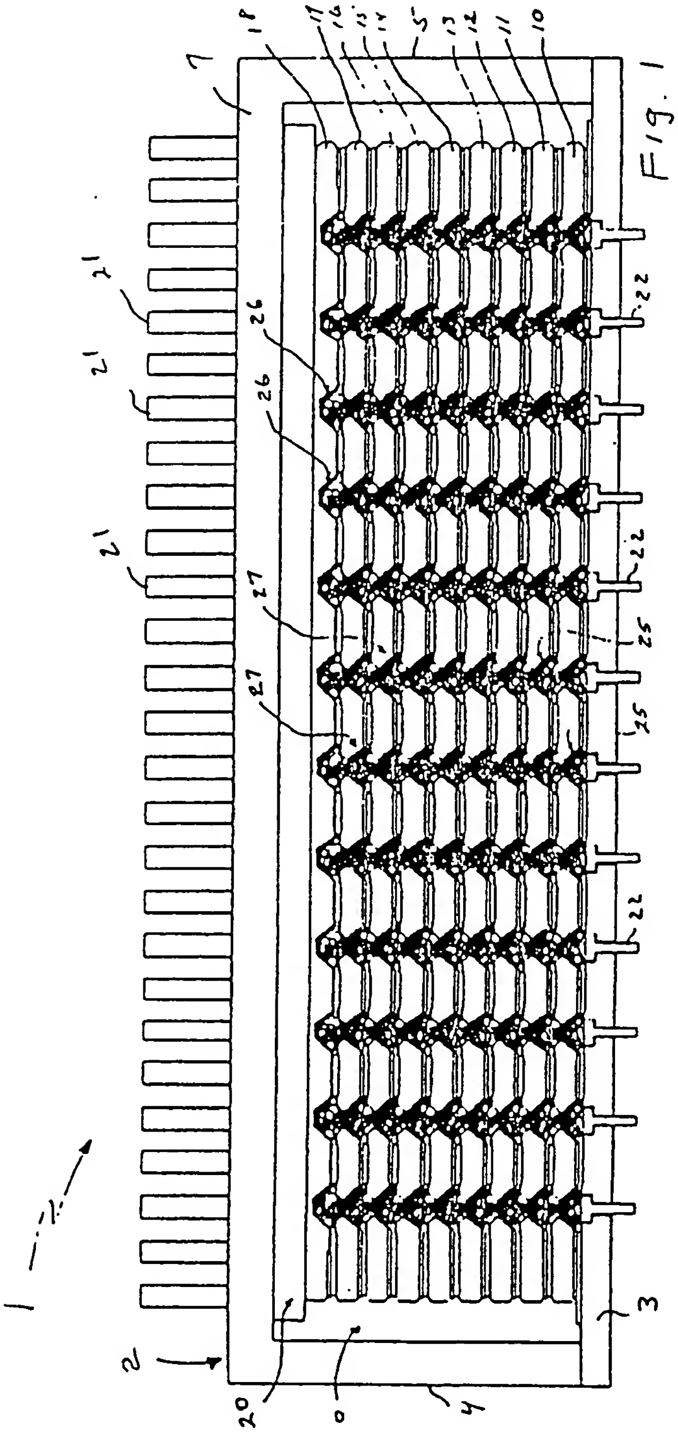


Fig. 1

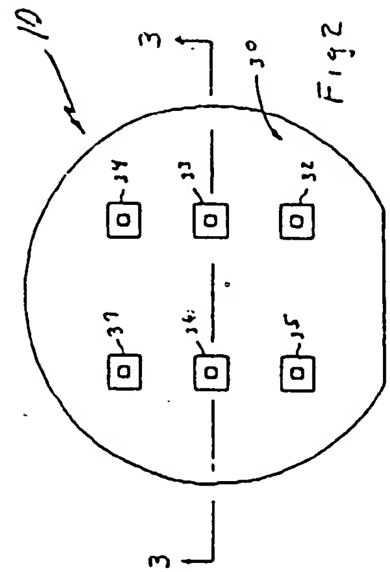


Fig 2

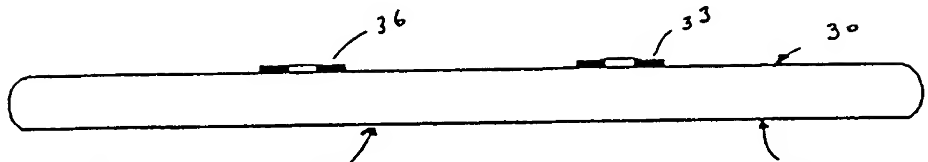


Fig 3

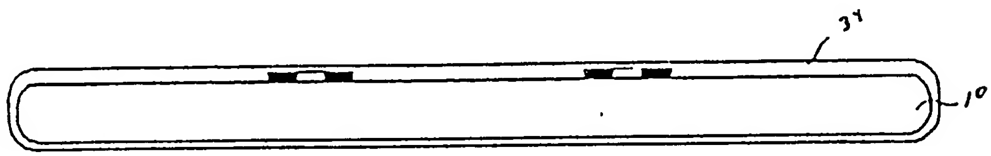


Fig 4

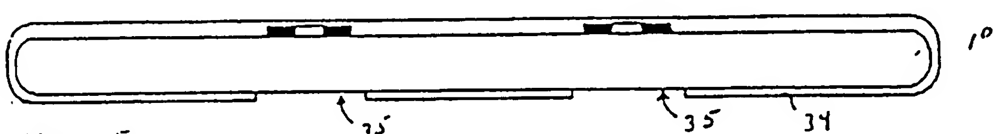


Fig 5

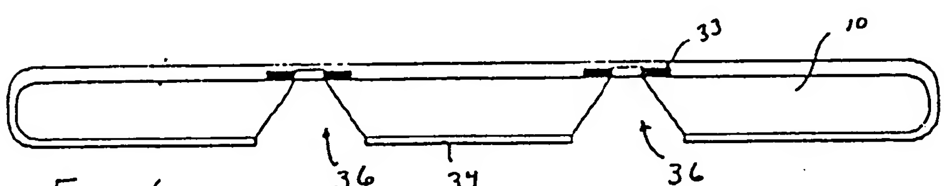


Fig. 6

Claims

1. A semiconductor wafer array characterised in that it includes a plurality of wafers (10-18) of semiconductive material which are stacked one on top of another, each of the wafers (10-18) having at least one via (25) which is in alignment with a via (25) in an adjacent wafer (10-18), the via (25) having a first end terminated by a first hole (41) in a first surface (30) of the wafer (10), a second end terminated by a second and relatively larger hole (42) in a second and opposite surface (31) of the wafer, and a constriction in the via (25) between the first (41) and the second ends (42); insulation means (40) for electrically insulating the exposed surface of the via between the first (41) and said second ends (42); an electrically conductive pad (33) surrounding the first hole (41) for making an electrical connection to electrical circuits located on the first surface (30); and an electrically conductive compliant material which is located in the via (25) and, when not compressed, extends outwardly beyond the plane of the first (41) and said second holes (42) for making an electrical connection with the electrically conductive compliant material in the via (25) located in the adjacent one of the plurality of wafers (10-18) when the adjacent wafer (11) is pressed against either the first (30) or the second surfaces (31).

2. An array according to claim 1 wherein the constrict on in the vias (25) in each of the wafers (10-18) restricts movement of the compliant material in the vias (25) through the first hole (41) when pressure is applied to the compliant material in the direction of the first hole (41).

3. An array according to claims 1 or 2 wherein the electrically conductive compliant material includes a cone-shaped portion.

4. An array according to any preceding claim wherein the electrically conductive compliant material comprises an elongated portion having substantially parallel side portions which extend from the apex of the cone-shaped portion.

5. An array according to claims 1 or 2 wherein the via (25) includes a section where the side walls are the shape of a truncated pyramid.

6. An array according to claims 1,2 or 5 wherein the via (25) comprises an elongated portion having substantially parallel side walls which extend from the truncated end of the pyramid-shaped side walls.

7. An array according to any preceding claim wherein the compliant material comprises a wad (27) of wire.

8. An array according to any of claims 1 to 6 wherein the compliant material comprises a compliant electrically conductive elastomer.

9. An array according to any preceding claim wherein the first surface (30) of each of the wafers (10-18) comprises a compliant electrically insulating material.

10. A semiconductor wafer array according to any preceding claim wherein the array further includes a housing (2) having base plate (3) and a top wall (7), the wafers (10-18) being stacked inside the housing (2) between and parallel to the base plate (3) and the top wall (7); a plurality of electrically conductive feed through pins (22) mounted in the base plate (3), so as to make electrical contact with the electrically conductive compliant material within the vias (25); and pressure means between the top wall (7) and the top wafer (18) to compress the wafers (10-18) and to produce an electrically conductive path between adjacent wafers (10-18).

11. An array according to claim 10 wherein the pressure applying means includes cooling means for conducting heat from stack of wafers (10-18) to the top wall (7).

12. An array according to claim 11 wherein the cooling means for conducting heat from the stack of wafers (10-18) to the top wall (7) comprises a compliant member (20) for compensating for thermal expansion and contraction of the stack of wafers (10-18).

13. An array according to claims 11 or 12 including means mounted in the top wall (7) and extending outwardly therefrom for dissipating heat from the top wall (7).

14. A method of making a semiconductor wafer array comprising the steps of: providing a plurality of wafers (10-18) of semiconductive material, each of the wafers (10-18) having a first (30) and a second surface (31) with an electrical circuit including an electrically conductive pad (32-37) having a central hole located on the first surface (30); providing a first hole having an inwardly directed side wall extending from the second surface (31) toward the first surface (30) in each of the wafers (10-18) beneath the pad (32-37); removing portions of the wall of the first hole for providing a second hole which diverges from the first hole to the edges of central hole of the pad (32-37) on the first surface (30) the first and said second holes combining to form a via (25); providing an electrically insulating layer (40) on the exposed wall surfaces of the via (25) in each of the wafers (10-18); inserting in each of the vias (25) produced by the exposing steps an electrically conductive compliant material, the material extending, when not compressed, beyond the plane of the ends of the vias (25); stacking the wafers one on top of the other so that the compliant material in a via (25) in one of the wafers (10-18) is in registration with the compliant material in the via (25) in an adjacent wafer (10-18); and compressing the adjacent wafers (10-18) together so as to compress the compliant material therebetween and thereby form an electrical circuit between the compliant material in the adjacent wafers (10-18).

15. A method of making a semiconductor wafer array comprising the steps of: providing a

plurality of wafers (10-18) of semiconductive material, each of the wafers (10-18) having a first (30) and a second surface (31) with an electrical circuit including an electrically conductive pad (32-37) having a central hole located on the first surface (30); coating the first (30) and the second surfaces (31) of each of the wafers (10-18) with an etch resistant material; patterning the etch resistant material on the second surface (31) of each of the wafers (10-18) so as to open a square area in the etch resistant material and expose the semiconductive material beneath the pad (32-37); exposing each of the wafers (10-18) to an anisotropic etch process so as to produce a first hole having an inwardly directed side wall extending from the second surface (31) toward the first surface (30) in each of the wafers beneath the pad (32-37); patterning the etch resistant material on the first surface (30) of each of the wafers (10-18) so as to open a square area in the etch resistant material and expose the semiconductive material within the centre of the pad (32-37); exposing each of the wafers (10-18) to a second etch process so as to remove portions of the wall of the first hole and produce a second hole which extends from the first hole to the etch resistant material in the centre of the square ring-shaped pad (32-37) on the first surface (30) in each of the wafers (10-18) beneath the pad (32-37) first and second hole combining to form a via (25) removing the etch resistant material from the first surface (30) of each of the wafers (10-18) so as to expose the square ring-shaped pad (32-37); providing an electrically insulating layer (40) on the exposed wall surfaces of the via (25) in each of the wafers (10-18); inserting in each of the vias (25) produced by the exposing steps an electrically conductive compliant material, the material extending, when not compressed, beyond the plane of the ends of the vias (25); stacking the wafers (10-18) one on top of the other so that the compliant material in a via (25) in one of the wafers (10-18) is in registration with the compliant material in the via (25) in an adjacent wafer (10-18); and compressing the adjacent wafers (10-18) together so as to compress the compliant material therebetween and thereby form an electrical circuit between the compliant material in the adjacent wafer (10-18) and the pads (32-37) surrounding each of the vias (25) in registration.

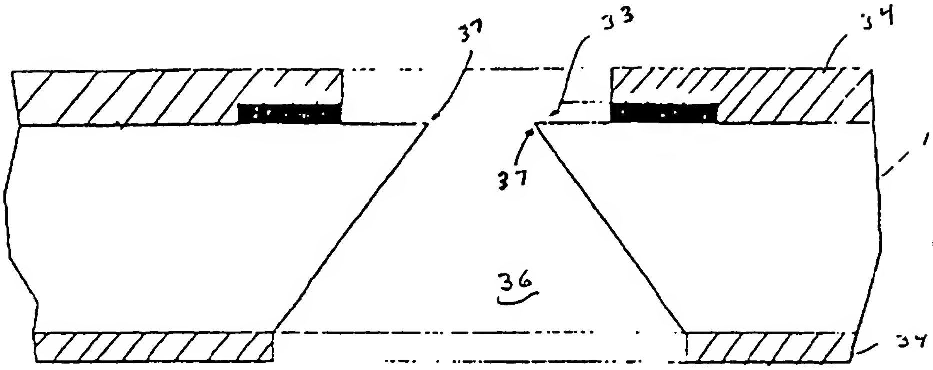


Fig 7

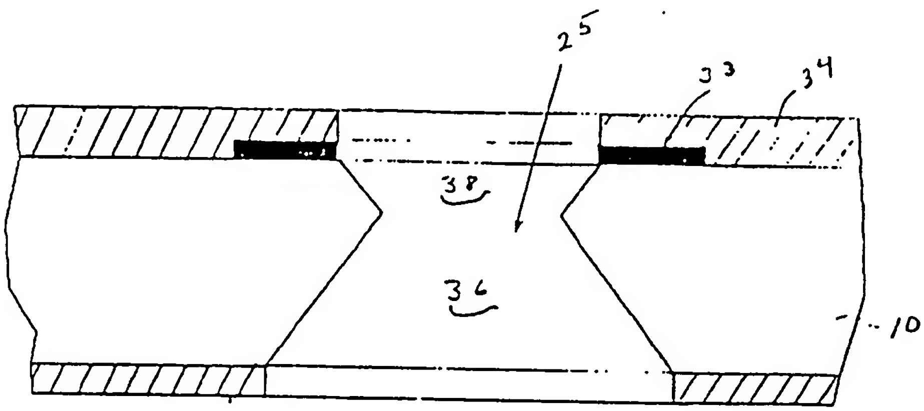


Fig 8

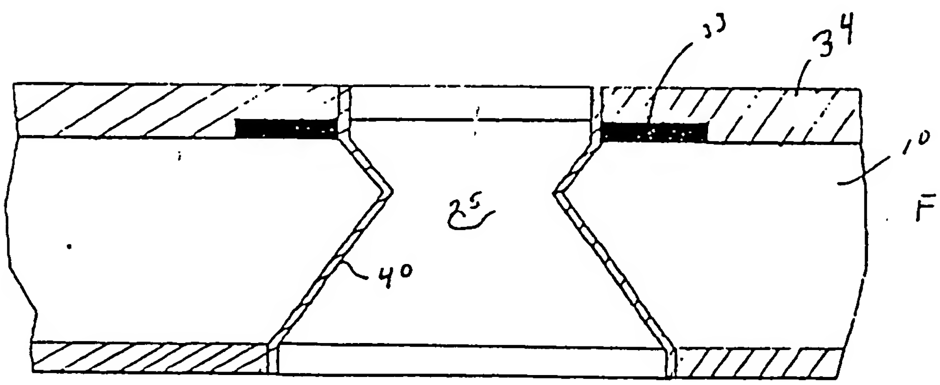


Fig 9

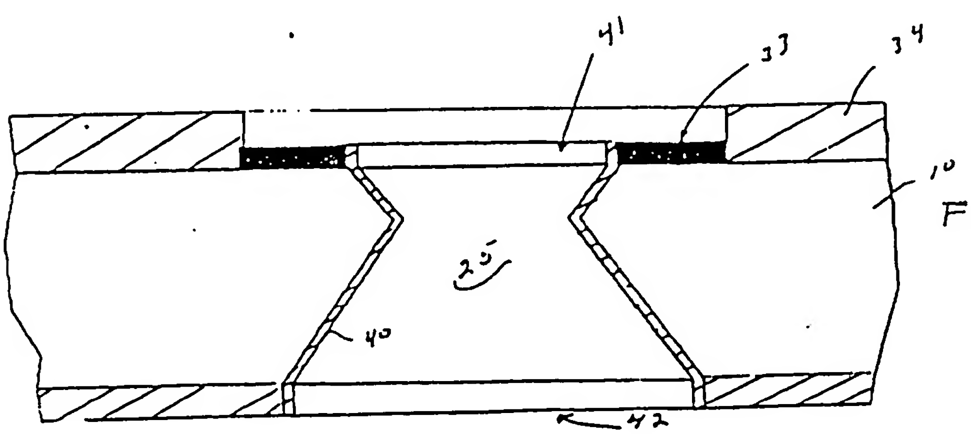


Fig 10

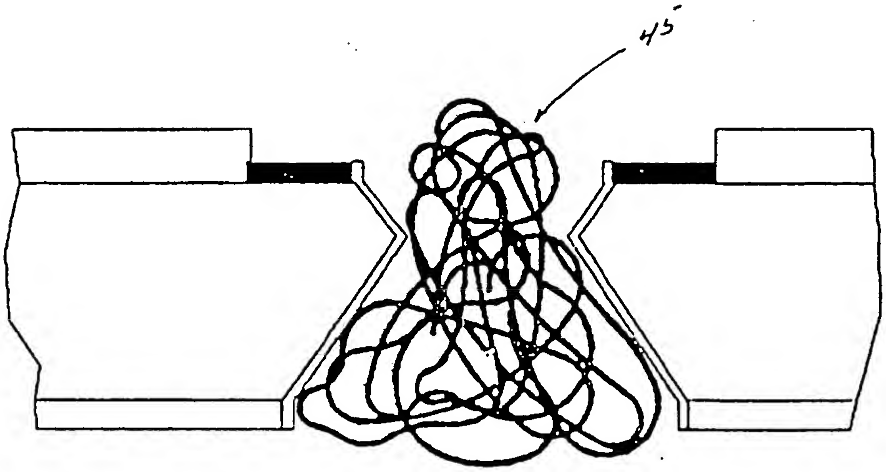


Fig 11

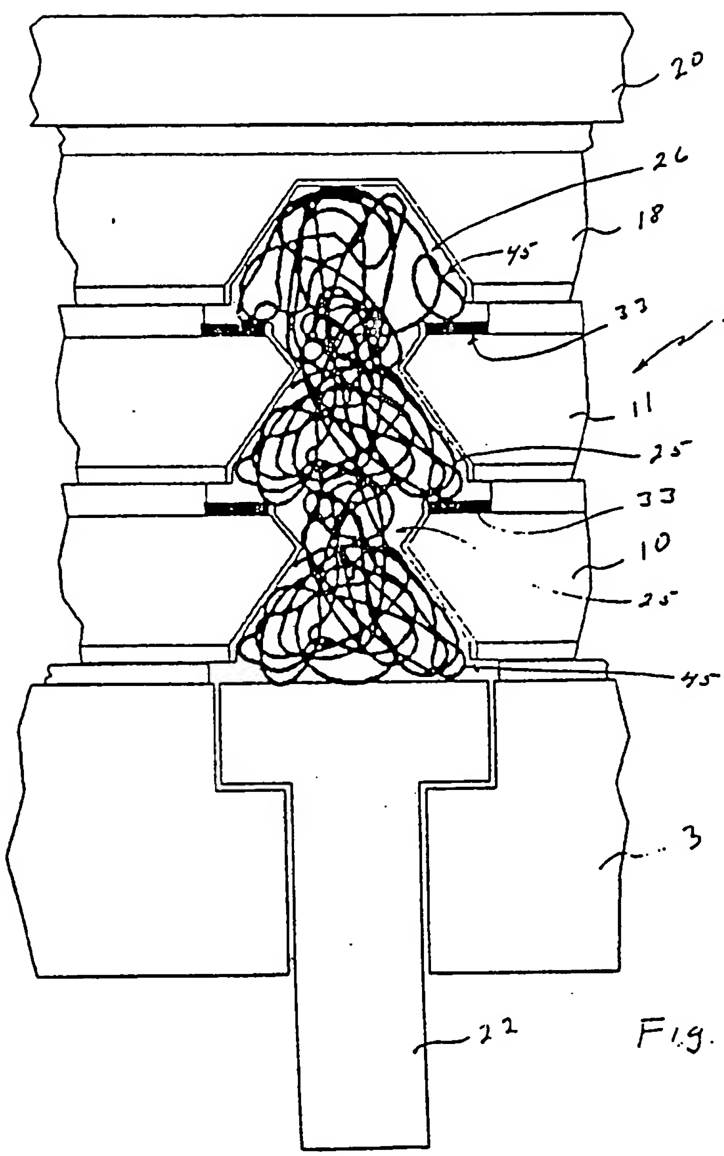


Fig. 12

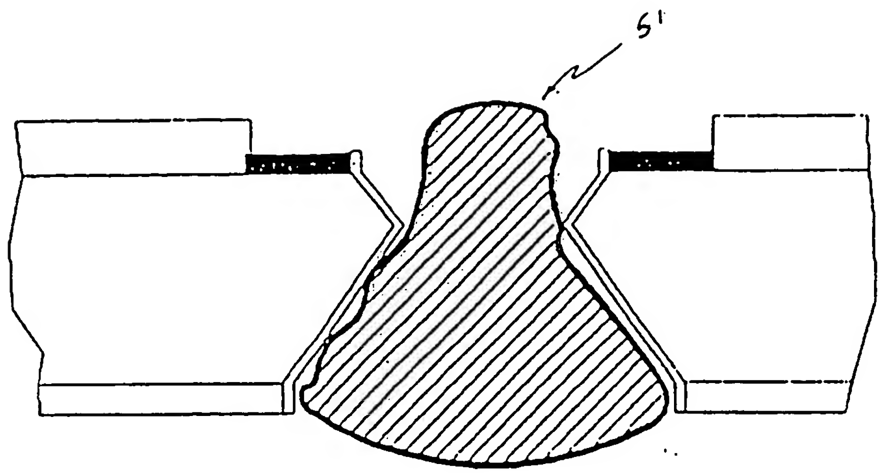


Fig 13

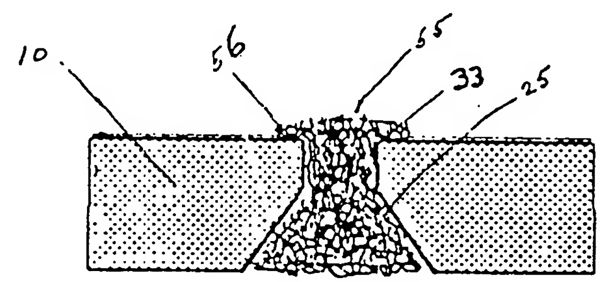
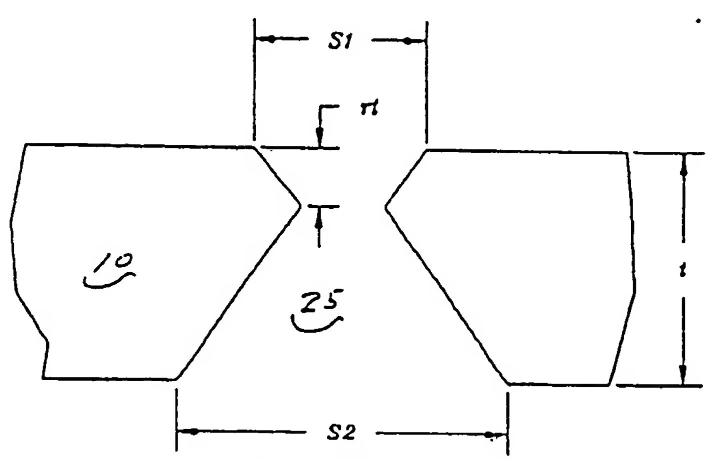


Fig. 14



$$S2 = S1 + \sqrt{2}\, t - 2\sqrt{2}\, rt$$

Fig 15

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 31 0029

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	DE-A-3 233 195 (MITSUBISHI DENKI K.K.) * Figures 2,5,7:; claim 1 * ---	1,10	H 01 L 25/08
A	GB-A-2 150 749 (STANDARD TELEPHONES AND CABLES PUBLIC LTD) * Figure 7; claims 1,16 * ---	1,4,14	
A	EP-A-0 206 696 (FUJITSU) * Figures 1,9,16; claim 1 * ---	1,13	
D,A	US-A-4 574 331 (TRW) * Column 4, lines 48-60 * ---	1,7	
A	FR-A-2 012 333 (IBM CORP.) ---		
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TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	03-01-1989	DE RAEVE R.A.L.

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